



PowerPro[®] MG

PowerPro MG is an automated memory power optimization solution that identifies Memory Gating opportunities based on Calypto's patented Sequential Analysis Technology. PowerPro MG takes advantage of the low-power modes available in today's on-chip memories to reduce both dynamic and leakage power. The tool reads in an RTL design and its corresponding memory models and generates new low-power RTL that looks identical to the original RTL with the addition of Memory Gating logic. The output of PowerPro MG is comprehensively verified with sequential equivalence checking to ensure no functional changes are introduced.

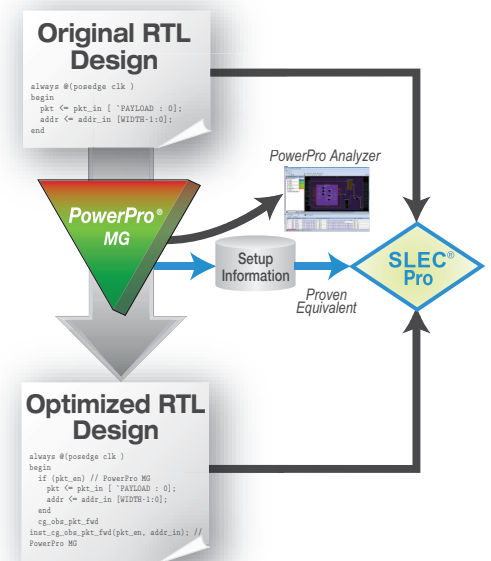
Memory Power Reduction through Memory Gating

PowerPro MG automates the identification and insertion of Memory Gating logic into the user's original RTL to dramatically reduce dynamic and leakage power. To reduce dynamic power, PowerPro MG evaluates circuit behavior across multiple clock cycles to identify Memory Gating opportunities to shut down the memory enable signal without impacting circuit behavior. PowerPro MG then automatically generates logic to control the memory enable signal to eliminate unnecessary memory accesses. In cases where logic already exists to control the memory enable signal, PowerPro MG can add additional logic to further eliminate memory accesses that are not required for correct functional operation.

The use of sleep modes in today's SoCs to reduce memory leakage power is generally relegated to situations when an entire block containing memories is put into an idle mode—that is, a mode when the block can be completely shut down without impacting the device's functionality. If a designer wishes to employ a more fine grained approach to using sleep modes on individual embedded memories, there are a number of complexities that need to be taken into account to ensure power is in fact reduced and design functionality is not impacted:

- Dynamic power vs leakage power: There is a trade-off between the dynamic power penalty associated with entering and exiting sleep mode and the savings associated with the memory being in sleep mode. The duration of the sleep mode must be sufficiently long for there to be actual power savings.
- Functional correctness: A memory can only be put into sleep mode when no memory accesses are required by the function.
- Timing specs need to be considered for Light Sleep mode entry/exit: The memory enable function (indicates when memory accesses occur) needs to be predicted so that the memory gating logic controls the memory to enter and exit sleep mode according to the timing spec requirements.

PowerPro MG reduces leakage power by automatically generating logic to control the sleep modes of individual embedded memories. Using sequential analysis to understand the functionality of the design across multiple clock cycles, PowerPro MG produces Memory Gating logic that guarantees the entry and exit from sleep mode meet the functional needs and timing spec of the device. This means that the memory gating logic ensures that the memory is out of sleep mode when accesses are required by the design and takes into account, in some cases, the need to begin exiting sleep mode several cycles prior to the next memory access. The trade off between the leakage power savings associated with sleep mode and the dynamic power penalty of entering and exiting sleep mode are taken into account by PowerPro MG through its



PowerPro MG reduces both dynamic and leakage memory power.

built in prototyping engine and sequential analysis capability. The tool automatically generates the memory gating logic to ensure that the use of sleep mode results in memory power savings.

PowerPro MG's built in prototyping engine also takes into account area and timing. Design trade-offs are made to select the memory gating logic that maximizes power reduction and ensures minimal impact to these key design parameters.

Benefits

- Eliminates wasted dynamic and leakage memory power
- Comprehensive, fully automated formal verification flow via SLEC Pro
- Reduces power with little or no impact on timing or area
- Produces clearly readable power optimized RTL
- Eliminates error prone manual RTL changes
- Optimized RTL fits seamlessly into existing RTL design flows
- Power savings are cumulative and complementary to downstream tools

PowerPro MG consistently produces better results, in orders of magnitude less time, than manual RTL Memory Gating. The new PowerPro MG generated RTL is comprehensively verified with formal equivalence checking to guarantee that no functional changes are introduced. No other solution provides this combination of automatic memory power optimization and formal verification. The power optimized RTL maintains cycle-accurate behavior at the block boundary. Therefore, existing simulation regressions can be used to verify PowerPro generated RTL.

Comprehensive Formal Verification

SLEC Pro provides comprehensive formal verification of the PowerPro MG generated RTL. SLEC Pro is Calypto's Sequential Logic Equivalence Checking product which compares the functionality of the original RTL design with the PowerPro MG optimized design for all possible input sequences, over all time.

PowerPro MG generates out a SLEC Pro setup script for automating the formal verification flow. This setup script contains all the TCL commands required to formally prove the PowerPro MG optimized RTL and original RTL are functionally equivalent.

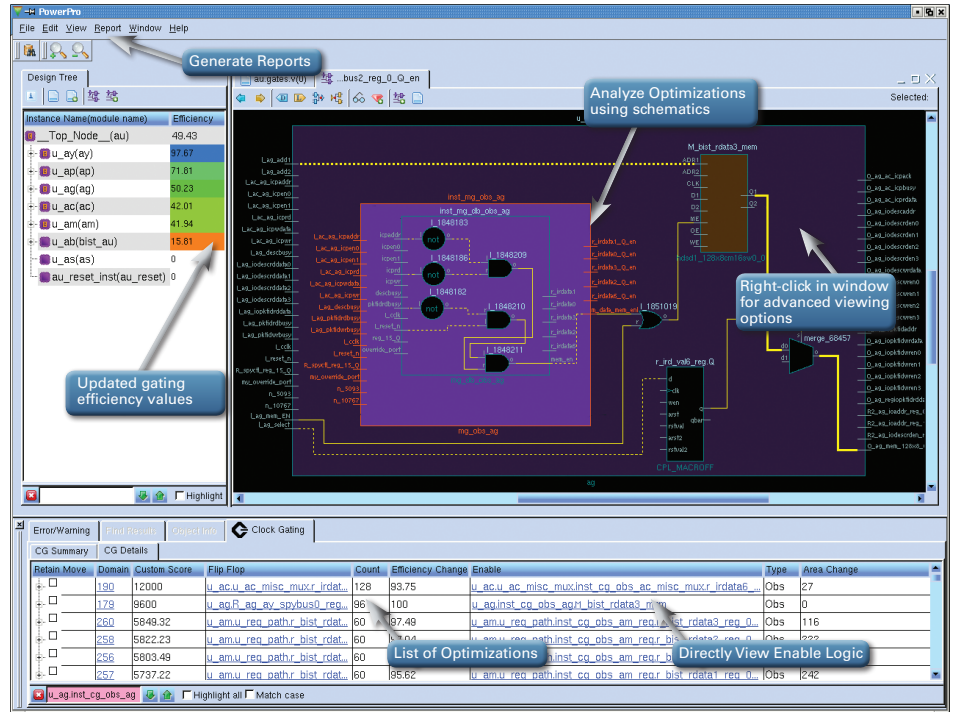
SLEC Pro is part of the SLEC product family which has been proven by dozens of customer on hundreds of designs to verify manual RTL optimizations like retiming, pipelining and clock gating.

PowerPro Analyzer

The PowerPro Analyzer is a powerful graphical visualization tool that provides a complete view of the PowerPro MG optimized designs. PowerPro Analyzer allows users to view power optimizations in the context of RTL source code, schematic display and design hierarchy. All design views are hyperlinked for rapid navigation and analysis of the optimizations generated by PowerPro MG, ensuring designers have detailed understanding of the optimizations PowerPro MG is performing.

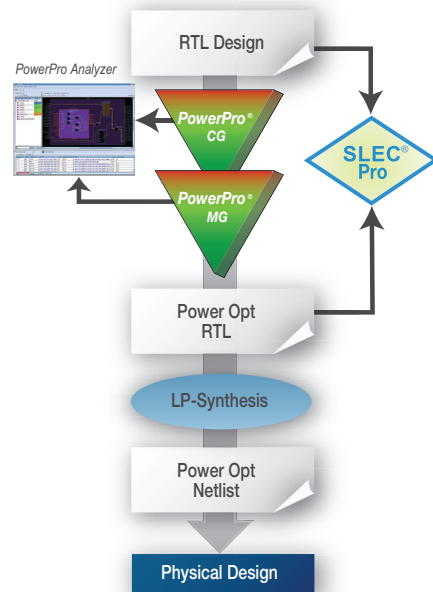
Fits into Existing Design Flows

PowerPro MG has been integrated into leading RTL synthesis tool flows. All the



PowerPro Analyzer provides a detailed view of the PowerPro MG memory power optimizations.

synthesis pragmas and verification directives are retained in the PowerPro MG generated RTL for synthesis and simulation.



PowerPro MG and SLEC Pro fit into existing design flows

PowerPro MG supports industry standard file formats including:

- Synthesizable RTL (Verilog or VHDL)
- Technology library files (.lib)
- Synopsys Design Constraints (SDC)
- Switching activity files (SAIF or VCD)
- Common Power Format (CPF)

PowerPro MG is controlled through a TCL command interface that is organized into three basic functions: setup, optimize and output. The setup commands specify the design, library, and constraint files. The optimize commands initiate sequential analysis on the design and generate memory gating logic. The output commands write out the PowerPro MG optimized RTL and SLEC Pro TCL script for automating the formal verification. The power savings produced by PowerPro MG is complementary and cumulative to downstream power reduction tools.

System Requirements and Compatibility

- Languages:
 - VHDL 87, 93 & 97 and Verilog 95 & 2001
- Operating Systems:
 - Redhat Enterprise Linux 3.0 and 4.0
- Platforms:
 - 32-bit and 64-bit x86 compatible hardware
- Memory:
 - 2 GB minimum

To learn more, visit www.calypto.com

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