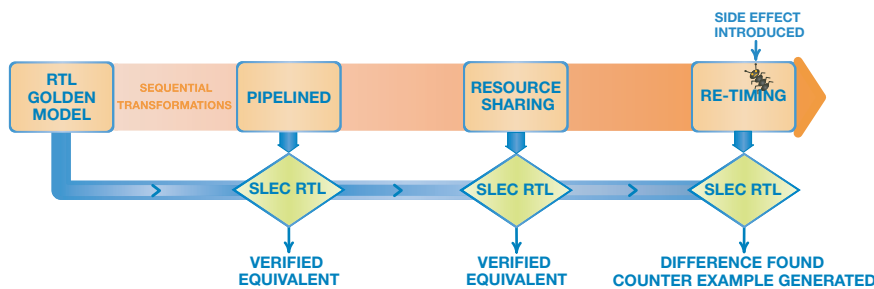


## SLEC RTL

# CALYPTO

SLEC™ RTL is the semiconductor industry's first sequential equivalence checker. SLEC RTL functionally verifies block-level RTL designs with sequential differences such as pipeline and state machine changes. SLEC RTL improves verification productivity and coverage when making micro-architectural optimizations for power, timing and area.



As RTL is refined for power, timing and area, sequential transformations are made to the original “golden” design. At each step in the refinement process SLEC RTL functionally verifies that the original hardware intent remains consistent or immediately identifies the difference.

### SLEC RTL OVERVIEW

SLEC RTL is a sequential equivalence checker that verifies functionality by comparing a RTL design specification against a “golden” reference design. If the designs are not functionally equivalent, SLEC RTL detects the design difference and immediately generates a counter-example for debug. SLEC RTL ensures functional correctness of micro-architectural optimizations, giving designers confidence and immediate feedback when making RTL changes.

Micro-architectural optimizations such as pipelining, resource sharing, retiming and clock gating are common sequential design changes. Sequential changes affect design state, throughput and latency which can invalidate existing testbenches and require additional manual test-bench validation. Because SLEC RTL can verify designs with sequential differences it can be used earlier in

the design process, extending the use of functional equivalence checking beyond gate-level design.

SLEC RTL verifies block-level RTL designs written in Verilog or VHDL. SLEC RTL does not require test benches or properties to verify your RTL design. Sequential equivalence checking complements full chip simulation by leveraging previous functional verification across all subsequent RTL changes. SLEC increases functional verification effectiveness and enables designers to find bugs that other methodologies miss.

SLEC RTL is part of Calypto's SLEC product family. The SLEC product family also includes the SLEC SYSTEM sequential equivalence checker which verifies RTL implementations against System C / C++ design specifications. SLEC SYSTEM is the only equivalence checker that supports sequential differences, word-level data abstraction and system-level languages.

### BENEFITS

- Provides design confidence when making micro-architectural optimizations by identifying functional differences in optimized circuits.
- Improves functional verification effectiveness without requiring additional testbenches or properties.
- Proves functional equivalence across levels of sequential and data abstraction.
- Increases timing optimization options by verifying re-timed and pipelined logic with comprehensive formal methods.
- Saves weeks of re-running system-level regressions by quickly detecting side effects.

### FEATURES

#### Enhanced Verification

SLEC RTL has a number of built-in consistency checks that guide development of high quality RTL for synthesis. SLEC RTL identifies design differences in short counter-examples that give designers immediate feedback so they can quickly resolve design issues. SLEC RTL enhances functional verification so designers can innovate with confidence and meet or exceed system specifications.

#### Sequential Analysis

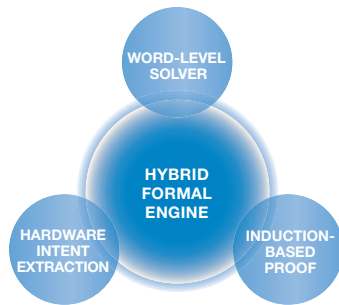
For complex chips such as micro-processors, detailed power, timing and area tradeoffs are not clear until each micro-architecture is characterized. SLEC RTL's powerful sequential analysis capabilities verify micro-architectural changes such as:

- Rebalancing long combinational logic paths across state elements

- Resource sharing or duplication
- Changes to pipeline datapath and control logic
- Clock gating such as sleep mode logic
- Interface protocol changes
- I/O throughput and latency differences

### Hybrid Technology

SLEC RTL is based on a hybrid formal engine that overcomes the technical limitations caused by the requirement of one-to-one flip-flop matching in current combinational equivalence products. SLEC RTL's patent pending hybrid engine combines three core technologies: word level solvers, induction based proof and hardware intent extraction. SLEC RTL is the result of over 30 man-years of on going Calypto development in state of the

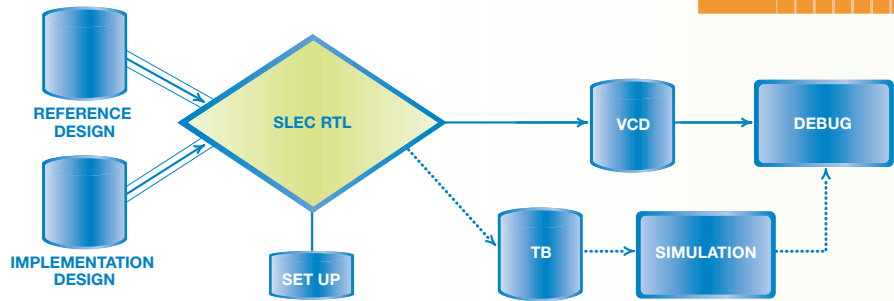


The underlying SLEC technology has three core engines to bridge data and sequential abstraction. This technology combines simulation and state of the art formal methods to perform sequential equivalence checking.

art functional verification technology.

### Modes of Operation

SLEC RTL has two modes of operation: bug detection mode and full proof mode. In bug detection mode SLEC RTL minimizes the time to find bugs by displaying differences in a short counter-example. Counter examples are typically 3-5 cycle/transaction VCD waveforms or simulation test-



Given reference and implement source code along with setup information to specify consistent initial states and I/O differences, SLEC RTL proves functional equivalence or identifies design differences. Design differences are represented as VCD files or simulation testbenches (TB) which can be used to debug and locate the source of design errors.

benches that can be run with common 3rd party simulators. In full proof mode, SLEC RTL deploys additional formal methods to inductively prove that designs are functionally equivalent for all time over all possible input sequences.

### User Interface

SLEC RTL is controlled through an intuitive Tcl interface that is similar to common simulation environments. Tcl scripts specify the source files, clocking, and reset state information for each design. In the case of designs with sequential differences, throughput and latency specification as well as differences in input and output mappings can be defined in the Tcl script. SLEC RTL Tcl features include:

- File specification using common Verilog file conventions and flags
- Hierarchy-based black boxing for modules or instances
- Constraints specification
- Save and restore of the verification database
- Mapping operations for design I/O alignment
- Temporal specification of design

reset, clocking and I/O

### Advanced Debugging Environment

SLEC RTL assists designers in locating functional differences in their designs. SLEC RTL debug capabilities provide thorough verification, which enables designers to find bugs missed by simulation, and reduces the time to catch side effects:

- Generates a VCD or testbench counter-example demonstrating the functional difference between the designs.
- Runs a design consistency check to ensure user setup correctness and detect common errors such as initialization, poorly formed clocking, gating, latch pipelines etc.

### SYSTEM REQUIREMENTS AND COMPATIBILITY

- **Languages:**  
VHDL 97 and Verilog 2001
- **Simulators:**  
ModelSim™, VCS™, NCSim™
- **Debuggers:**  
Debussy™, SignalScan™
- **Operating Systems:**  
Linux Redhat 7.2 and Enterprise 3.0
- **Platforms:**  
32-bit Linux
- **Memory Requirement:**  
2 GB
- **Disk Space (For installation):**

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